SECTION I—CLAIMS

Amendment to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application. Claims 1-3, 6-11, 24, and 29 are amended herein. Claims 4-5, 12-13, 15-17, 19-20, 23, and 25-27 remain canceled herein without prejudice. No new claims are added.

Listing of Claims:

1. (Currently amended) A non-transitory processor readable medium having instructions stored thereon that, when executed by a processor in a switch, cause the switch to perform a method for implementing one or more packet modification operations on a packet received at the switch, wherein the method comprises:

associating a data structure link with the packet received at the switch by inserting a data structure index corresponding to the data structure link into a header of the packet;

retrieving a data structure from memory of the switch via the data structure link associated with the packet, wherein the data structure comprises:

a first pointer to a sequence of commands for execution by a processor of the switch to implement the one or more packet modification operations stored in packed format with more than one command stored in a single addressable entry in a sequence in a first memory area of the memory, and

a second pointer to a burst of data or mask items stored in packed format with more than one data or mask item stored in a single addressable entry in the stored burst in a

second memory area of the memory distinct from the first memory area, the burst of data or mask items for use by the processor in executing the one or more commands;

retrieving the commands in the sequence from the first memory area via the first pointer;

retrieving the data or mask items in the burst from the second memory area via the second pointer; and

performing one or more packet modification operations on the packet by executing the commands in the sequence via the processor using the burst of data or mask items as operands or masks for operands in the one or more packet modification operations performed.

2. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first and second memory areas are located in different memories.

3. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first and second memory areas are located in the same memory.

4-5. (Cancelled).

6. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

7. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip in relation to the processor.

8. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip in relation to the

processor.

9. (Currently amended) The non-transitory processor readable medium of claim 1 wherein the data structure comprises a plurality of pointers, each to a sequence of commands implementing one or more packet modification operations.

10. (Currently amended) The non-transitory processor readable medium of claim 9 wherein the data structure comprises a plurality of pointers, each to a burst of data or mask items.

11. (Previously presented) A method within a switch for performing one or more packet modification operations on a packet received at the switch, wherein the method comprises:

associating a data structure link with the packet received at the switch by inserting a data structure index corresponding to the data structure link into a header of the packet;

retrieving a data structure from memory of the switch via the data structure link associated with the packet, wherein the data structure comprises:

a first pointer to a sequence of commands for execution by a processor of the switch to implement the one or more packet modification operations stored in packed format with more than one command stored in a single addressable entry in a sequence in a first memory area of the memory, and

a second pointer to a burst of data or mask items stored in packed format with more than one data or mask item stored in a single addressable entry in the stored burst in a second memory area of the memory distinct from the first memory area, the burst of data or mask items for use by the processor in executing the one or more commands;

retrieving the commands in the sequence from the first memory area via the first pointer;

retrieving the data or mask items in the burst from the second memory area via the second pointer; and

performing one or more packet modification operations on the packet by executing the commands in the sequence via the processor using the burst of data or mask items as operands or masks for operands in the one or more packet modification operations performed.

12-13. (Canceled).

14. (Previously presented) The method of claim 11 wherein the first and second memory areas are:

located in different and distinct physical memories;

located in distinct portions of a same physical memory;

located in an internal recipe RAM (Random Access Memory) and an external SRAM (Static Random Access Memory) respectively;

located in a memory implemented off-chip from a modification processor to execute the sequence of commands; or

located in a memory implemented on-chip with the modification processor to execute the sequence of commands.

15-17. (Cancelled).

18. (Previously Presented) The method of claim 11 wherein the data or mask items in the burst comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

19-20. (Cancelled).

21. (Previously presented) The method of claim 11 wherein the data structure comprises a

plurality of pointers, each to a sequence of commands implementing one or more packet modification operations.

22. (Previously presented) The method of claim 11 wherein the data structure comprises a plurality of pointers, each to a burst of data or mask items.

23. (Cancelled).

24. (Currently amended) A packet modification system comprising:

an associator to associate a data structure link with a packet received at the packet modification system by inserting a data structure index corresponding to the data structure link into a header of the packet;

a physical memory to store a data structure comprising:

a first pointer to a sequence of commands implementing one or more packet modification operations and stored in a first memory area of the physical memory in packed format with more than one command stored in a single addressable entry in the stored sequence, and

a second pointer to a burst of data or mask items stored in a second memory area of the physical memory distinct from the first memory area in packed format with more than one data or mask item stored in a single addressable entry in the stored burst; and

a processor to:

retrieve the commands in the sequence from the first memory area via the first pointer;

retrieve the data or mask items in the burst from the second memory area via the second pointer, and

execute the commands in the sequence using the burst of data or mask items as operands

or masks for operands in the one or more packet modification operations.

25-27. (Cancelled).

28. (Previously presented) The system of claim 24 wherein the first and second memory areas are located in different memories.

29. (Currently amended) The system of claim 24 wherein the first and second memory areas are located in the same physical memory.

30. (Previously presented) The system of claim 24 wherein the processor comprises a pipeline processor core to retrieve the commands in the sequence in a first stage, and execute the commands in the sequence in one or more subsequent stages.